evatec
process systems

EDITION 6

LAYERS

Extracts from LAYERS 6

Ralph Zoberbier
Head of BU Advanced Packaging

ADVANCED PACKAGING

A true enabling technology for next generation electronics and megatrend applications

ADVANCED PACKAGING SEMICONDUCTOR OPTOELECTRONICS PHOTONICS

ADVANCED PACKAGING NEWS

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A true enabling technology for next generation electronics and megatrend applications

The year 2020 will certainly be remembered in all of our minds as a point in history that truly changed so many people's home and work lives from one day to the next. Enhanced digitalization in all areas of our lives is seen as a key enabler to develop a better, safer and healthier existence. The ongoing challenges and geopolitical changes push the electronics and semiconductor industry to increase global capacity at a tremendous speed, and to complete new technologies enabling applications like 5G, artificial intelligence, internet of things, autonomous and electrical driving. Advanced Packaging is more than ever one of the technology drivers to realize these enhancements. Evatec is at the forefront, offering innovative and latest state-of-the-art technologies in thin film deposition applications. In this issue you will find exciting articles about market and technology trends and achievements by our customers. In 2021 we will continue to focus on new products and solutions on wafer and panel level, and will continue to collaborate closely with our customers, partners and friends.

insights
Advanced Packaging

Ralph Zoberbier, Head of BU Advanced Packaging answers questions on the role of the industry going forward, the challenges it faces and how Evatec can contribute.

Q. You had already spent 20 years in Advanced Packaging when you joined Evatec at the end of 2019. It looks like you plan to stay in this industry for many more years. What makes you so excited about the industry and its technologies?

Advanced Packaging was introduced and established in the supply chain of electronics as a key enabler for next generation devices since its early days.

I started my career around 20 years ago when C4 bumping and Wafer Level Packaging were just being rolled out into high volume manufacturing for leading edge applications like the SONY PlayStation 2, both on ICs and Memory. Ever since then, Advanced Packaging technologies were supporting the never ending trends for smaller, lighter, thinner and more powerful devices. Mobile phones, and the transition into smartphones as we know them today, were only possible with the implementation of Advanced Packaging technologies on mission critical chips. However, Advanced Packaging always followed the front-end technology roadmap and Moore's Law. What really excites me however is that as front-end technology enhancements become more and more limited and extremely costly, Advanced Packaging really turned into a true enabling technology to shape our future.

Functionality and complexity is transferred from the chip into the package, which is no longer now a single chip package but rather a complete system in package, that delivers outstanding performance at reasonable costs. What could be more exciting than working with our passionate engineers, customers and industry partners on new technologies that support the mega trends of our century and help create new artificial intelligence, data storage concepts and greater computing power.

Q. What are the key market trends that drive innovation in Advanced Packaging technologies?

Mega trends are powerful, transformative forces that impact or even change the global economy, business and society. I believe the key trends that most impact Advanced Packaging are seen in areas like connectivity, health, safety, globalization and mobility. In all cases new improved electronic devices are needed to make the next step forward.

One of the key driving forces is certainly the implementation of 5G as a new communication standard. New infrastructure and the development of compatible next generation smartphones will be needed that support high volume data streams and higher communication speeds. Even in the challenging year of 2020 with its global pandemic, preparations of the supply chain continued full steam ahead and new manufacturing lines were established. Smartphone demand is expected to get back to pre pandemic levels in 2021 and beyond fueling the demand for Advanced Packaging.

New technologies in the automotive area will also drive semiconductor and its packaging applications. Smart automobiles are already a reality that support autonomous driving and other driver assisted features. The global push to electrical cars is another good example. One can easily see that the silicon content of cars is growing continuously with increasing demand for computing power and data storage, coupled with the most demanding requirements for electronics reliability and strong energy savings.

Last but not least, mega trends are fostering developments of new applications and products in areas like Artificial Intelligence, Internet of Things and Cloud Computing. Those applications have in common that they generate a great amount of data that needs to be computed and processed in real time and in parallel. This typically requires high speed data storage and transfer with the highest computing power. New chip designs and new system in package concepts support those requirements. Especially in those areas, new front-end nodes like 5nm and 3nm go hand in hand with new heterogenous integration technologies like Chiplets and SiP. Huge growth in demand in this Advanced Packaging segment is expected over the next 3-5 years.

Key market trends that drive innovation in Advanced Packaging technologies

Next Gen Smartphones
Miniturization & 5G

- Application processor SoC from 10nm to 7nm technology with first adoption of fan-out technology (InFo) vs. laminate substrate
- Drives continuous adoption of WLP, FOWLP & System in Package (SiP)
- 5G will require more complex & multifunctional RF modules

Automotive
Electrification & AV

- Increasing SC content for Autonomy, Electrification & Connectivity
- Radar, Microcontrollers & Analog applications will require packaging developments for increased density, higher frequency, higher power & EMI shielding

High performance Computing
High density interconnect & heterogenous integration

- 5G, AI-Big Data drive technology development and market introduction of Chiplets
- Robotics, transportation, healthcare
- Strong demand for HBM integration

WLCSP & Fan-out (WLP & PLP)

- Wide adoption for PMIC and RF
- New potential for high-density Fan-out for APs and heterogeneous integration (CPU, memory)
- Push to FOPLP as supporter of cost reduction roadmap and heterogeneous integration
- Panel sizes up to 600mm x 600mm

Heterogeneous integration

- Si interposer adoption with TSVs
- Bump pitch reduction down to 10µm
- High-density substrate technology
- Fine line RDL
- High frequency, high signal integrity
- Separation of data and power lines
- Backside metal for advanced heat dissipation

Advanced IC substrates
(including embedded die packaging)

- Fine line interconnects with roadmap to 2µm L/S in 2022
- Embedded die technologies
- FO on substrate / RDL interposer
- Panel sizes typically 510mm x 515mm
- PVD becomes crucial to support roadmap as chemical Cu alternative

Q. Where do you see the technology going and what is Evatec's vision in Advanced Packaging?

Let me focus on the three most important technology segments that we believe are driving developments and new products.

Fan-out wafer level packaging (FOWLP) was introduced in the market around 10 years ago and was designed to provide better form factors, thermal and electrical performance and to increase the number of contacts without increasing die sizes. The adoption of FOWLP is still gaining momentum, and we currently see three trends that drive the technology at its core:

- New applications like Application Processors or Multi Die Packages require multi layer RDL, high density FO interconnects with features sizes down to 2µm L/S. New passivation materials and manufacturing technologies are required to support this trend.
- Secondly, the transition from wafer level to panel level processing is a fundamental change for Fan-out technology. Mounting pressure for cost reduction combined with increasing package dimensions are the key reasons that panel processing has been under investigation for some time by the packaging industry and its finally now coming to market. This requires panel capable process solutions and equipment which did not existing in the industry until now.
- Last but not least, Fan-out with its capability to combine multiple chips in one molded package is a key enabler to realize heterogenous packages without costly TSV and interposer technologies. Thin film RDL are manufactured on substrates, either wafer or panel scale. Known good dies are attached on this layer and finally molded to create the final package.

Heterogenous integration itself is another area that gains a lot of traction. It refers to the integration of separately manufactured components into a higher-level assembly. Under this theme, a wide range of different package designs and technology combinations are used to create high performance system solutions on a package level. This can include variations of Fan-out packaging, micro bumping, TSV, glass interposer and RDL interposer technologies. Many different manufacturing technologies play a significant role, most importantly die to die, wafer to wafer bonding and hybrid bonding to build the system. Additional enhanced back side metal layers are needed as effective heat dissipation layers for the systems. Each of the packaging techniques bring its own requirements and challenges while the true complexity comes from their combination.

Finally, I see new requirements in substrate technology such as fine line features and the integration of embedded components as a key trend that impacts Advanced Packaging. New complexity and functionality are being embedded into the substrate like interconnect bridges between different chips, i.e. a GPU and memory chips. In this way the substrate itself becomes a true technology piece of the overall package and component. These new requirements drive the adoption of non PCB manufacturing technologies like PVD and enhanced lithography solutions on a panel scale. OSATs and substrate contract manufacturers have recognized this new business opportunity and are fighting for their position in the market.

Evatec aims to be one of the leading equipment and process solutions in thin film deposition and is supporting our customers and partners in these exciting segments with leading edge technology, both on wafer and panel level. We believe that new levels of performance in regard to Rc performance, particle count, handling capability and productivity will help to bring new products to the market quickly. Tailored solutions for each application are needed to fully meet our customers' needs and expectations. Besides technology, effective customer support with strong local service organizations including application and process support are key focus areas in which we continuously want to extend and improve our performance.... and yes, we want to be a selected partner in each high-end packaging fab.

Q. What do you see as the biggest challenges faced by the Advanced Packaging industry in the next 5 years? How can Evatec play its part in solving them?

We clearly can see that Advanced Packaging is changing gears from a rather cost and formfactor driven technology to a real technology enabler. For decades, device manufacturers introduced higher performance products based on higher transistor density technology. However, this became more and more complex and costly, so packaging offers a solid alternative to bring complexity and functionality from the chip into the package. This pushes manufacturing technologies to a new level. Bump pitches will move to 20 or 10um on leading edge products, package sizes will increase significantly, and different material compositions will have to match to name just a few. This means that the supply chain, and especially equipment manufacturers, have to bring up new models that are rather "front-end like" tools at reasonable cost levels. As recently presented by INTEL at one of the leading industry conferences, panel based packaging

> "Evatec aims to be one of the leading equipment and process solutions in thin film deposition and is supporting our customers and partners in these exciting segments with leading edge technology, both on wafer and panel level"

is becoming a real "must have" and it's only a matter of time. Evatec is focused on key developments to provide the industry with highly reliable tools that meet particle specs and uniformities and are compatible with different materials and substrates. With our newly developed panel platform, we are ready today to help customers get their new lines up and running quickly.

In addition, I strongly believe that the right support infrastructure and Business Unit setup is crucial to meet the industry's expectations for quick and efficient support. The magic word is "Globalization". We are building up very strong local teams in our sales and service organizations to serve our customers with quick responses and solid process know-how. We also established a strong global team that shares information and comes up with solutions as quick as possible. The headquarters and the dedicated Evatec Competence Lab (ECL) focus on core technology and product development and is equipped with latest equipment generations to support development, sample requests and small volume manufacturing. All in all, I believe that Evatec is well prepared, especially in the key areas like FOWLP, Heterogenous Integration and Panel Level Packaging.

Q. What are the latest achievements that you want to share with us and what can we expect from Evatec Advanced Packaging Business Unit in 2021?

2020 was a very special year for all of us. The global pandemic was a clear low light in many regards. However, the Advanced Packaging Business Unit can look back to a very successful and positive year. Based on our flagship product, the HEXAGON, we could gain quite some market share in Flipchip and Fan-out applications at our key target customers. The first installations of the panel cluster tools in pilot production lines were a key milestone for the company but also the industry. I am excited to see this becoming a game changer in the packaging industry and I am happy that our company is an important part of this technology. In 2021 we have solid plans to launch new product generations to support our customers in the area of HD Fan-out, Heterogenous Integration and Next Gen IC substrates. There has never been a more exciting time to be in the packaging industry.

Electronics Packaging - From Afterthought to Product Differentiator

Industry guru, **Steffen Kroehnert**, shares his thoughts on the Advanced Packaging Industry and the emerging opportunities for Foundaries, IDMs and Suppliers.

Electronics packaging is generally divided into three major areas, Traditional Packaging - also called standard or mainstream packaging, and sometimes even just "Others" -, Advanced Packaging and Emerging Packaging Technologies.

Traditional Packaging is everything with wire or ribbon bond interconnects on ceramic, metal lead frame or organic laminated substrates, and it is typically a single die packaged. Advanced Packaging starts with Flip Chip interconnects (bumps, micro-bumps, Cu-Pillars), mainly on organic laminated substrates and has been growing during the last decade more and more into Wafer Level Packaging (WLP), which is Fan-in packaging with thin film processed RDLs (Redistribution Layers), Fan-out packaging on Wafer and Panel Level (Chip First - RDL Last, or RDL First - Chip Last, Face-up and Face-down approach), so called 2.5D interposer technology with Thru Silicon Via (TSV) with passive or more recent also active interposer, 3D Packaging such as die stacking, package stacking with Thru Package Via (TPV, which can be pre-formed or post-formed and e.g. Thru Mold Via (TMV), or Thru Glass Via (TGV)), 3DIC with TSV (via first, via middle and via last concepts), System-in-Package (SiP), and many different combinations of those, which are summarized under the term Heterogeneous Integration.

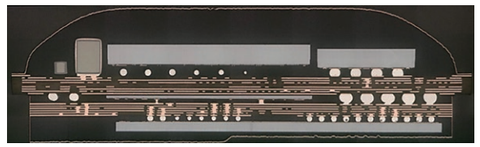


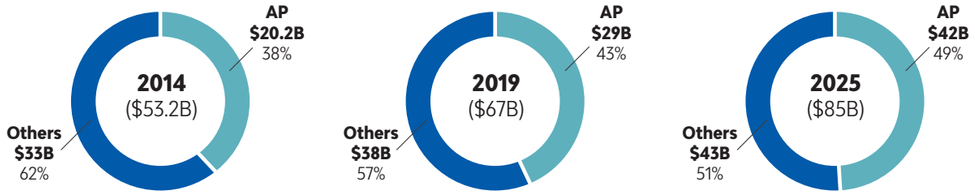
Figure 1: Highly Integrated 3D-SiP: Apple AirPods Pro SiP Cross-Section.

HETEROGENEOUS INTEGRATION ROADMAP

Under the title "**Heterogeneous Integration Roadmap (HIR)**: Driving Force and Enabling Technology for Systems of the Future", the executive summary of the roadmap talks about the vision of the HIR, which is available to everyone. "It became one of the most important roadmaps in the semiconductor world, after the International Technology Roadmap for Semiconductors (ITRS) was discontinued. The SIA7 (Semiconductor Industry Association) brought the ITRS to closure in July 2016, but we are now in a new world order with changes and disruptions that we could never have imagined before. The executive summary continues... "the need for roadmapping has never been clearer. The business landscape is experiencing great change with the continued rise of technology companies that are driving social media, cloud computing, search, online commerce, and big data, leading to integrated hardware-software driven applications and unprecedented growth of application spaces".

Looking at the Electronics Packaging market, we are seeing fast growth and new chances. The chances are not only for the typical players in this market, the OSAT, IDM and EMS companies, but also for Foundries and Material Suppliers stepping up in the value chain, and taking over an increasing share of the Advanced Packaging market. According to Yole Développement in France, the total packaging market is predicted to grow from $53.2B in 2014 to $85B in 2025. Advanced Packaging is going to count for 49% of that, coming from 38% in 2014. That is just an 11% higher share, but as the total packaging market is growing, the revenue in Advanced Packaging is predicted to more than double from $20.2B in 2014 to $42B in 2025. In 2019, wireless communication and consumer applications generated 85% of Advanced Packaging revenue.

Figure 2: Advanced Packaging Landscape in Post-COVID Economy - Live Market Briefing" Yole Développement, July 16, 2020.



Also, the traditional packaging market revenues are going up by more than $10B from $33B in 2014 to $43B in 2025. It is just its share in the total packaging market, which is growing as a whole, that is predicted to decrease by 11% from 62% in 2014 to 51% in 2025.

The COVID-19 pandemic impacted packaging revenues heavily. However, the revenue reductions of around 7% in 2020 are expected to be followed by a strong recovery in 2021 with around 14% growth. The traditional packaging market suffered more with a revenue drop of around 15% in 2020.

The main drivers for Advanced Packaging are the new mobile communication standard 5G, Artificial Intelligence (AI) and Deep Machine Learning combined with "Big Data" and High Performance Computing (HPC) in data centers, as well as the Internet of Things (IoT). Another driver bringing more value to Advanced Packaging is the fact that monolithic integration in System-on-Chip (SoC) slowed down and with it the realization of the so called "Moore's Law", an economic observation made by Gordon Moore, CEO and Co-Founder of Intel, in 1965. He prdicted the number of transistors in a dense Integrated Circuit (IC) was going to double every year for at least one decade, which he revised in 1975 to every two years. After "More Moore", the "More than Moore" technologies are increasingly required to continue "Moore's Law" at system integration level, and those are mainly Advanced Packaging technologies. That is also the main reason for Compound Annual Growth Rates (CAGR) 2019-2025 of 12.3% for Fan-out Wafer- and Panel Level Packaging (WLP/PLP), 5.9% for Flip Chip, 1.3% for Fan-in WLP, 25% for 3D Stacking (includes portion of wafers not included in Flip Chip or Fan-in WLP as used for pre and/or postprocessing around the 3D Stacking), and 17% for Embedded Die.

In terms of processed wafers, the largest portion in the Advanced Packaging market (2019 vs. 2025) is still Flip Chip (75% vs. 71%), followed by Fan-in WLP (12% vs. 9%), 3D Stacking (7% vs. 12%), and Fan-out WLP/PLP (6% vs. 8%). Despite the impressive CAGR of Embedded Die stated before, its share in the Advanced Packaging market stays below 1% as the total number of processed wafers is growing in this time frame with a CAGR of 7% (29M vs. 43M).

TSMC is showing in their "3D Fabric" concept "Advanced Packaging (BE 3D)" technologies as InFO (Integrated Fan-out), a Chip First approach with different options such as InFO-R and InFO-L, and CoWoS® (Chip-on-Wafer-on-Substrate), a Chip Last approach with different options such as CoWoS®-S, CoWoS®-R and CoWoS®-L.

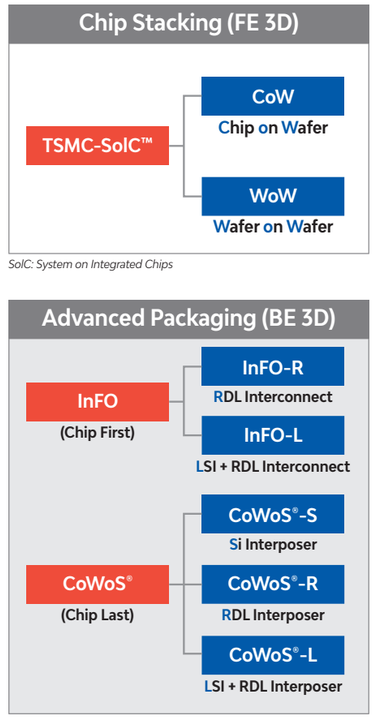
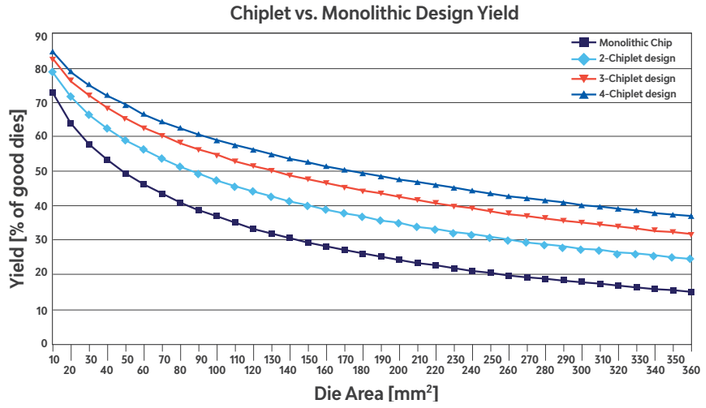


Figure 3: 3D Fabric™ Overview with FE 3D and BE 3D Solutions (Source: TSMC).

Figure 4: Wafer yield [%] in dependency on die size [mm²] on wafer (Source: WikiChip).



But wait, wouldn't we expect the names of the large OSAT companies like ASE Group, Amkor Technology, JCET Group, PTI, Tongfu Microelectronic or Tianshui Huatian Microelectronics here? TSMC is a Foundry, and that they are strongly involved in Advanced Packaging is underlining a trend when it comes to WLP. More IDMs and many Foundries are entering into that business taking a share from the OSATs. The reason is easy to understand. Advanced packaging technologies are getting closer to wafer fab processes, using wafer fab equipment, require clean room classes as used in wafer fabs due to the smaller features sizes such as RDL line width, spacing and thickness, via sizes and height, and contact pad pitches. The package is becoming a functional part of the product, chip-package-board co-design and co-development is essential, CPI (chip-package-interaction) considerations are crucial elements.

Looking at the revenues coming from its packaging business, TSMC would be the 4th largest OSAT in the world with an Advanced Packaging revenue of $2.88B in 2019, and business is continuing to grow. Back in June 2020, TSMC announced plans to invest $10.1B in building a new chip packaging and testing facility in Miaoli, northern Taiwan. The completion of the plant is scheduled for May 2021 with operations set to start mid of 2021.

Emerging packaging technologies are D2W (Die-to-Wafer) bonding and W2W (Wafer-to-Wafer) bonding with interconnects formed by TCB (thermo-compression bonding) or hybrid bonding, typically Cu pad to Cu pad without extra interconnect elements. TSMC is calling this in their "3D Fabric" concept "Chip Stacking (FE 3D)" SoIC™ (System-on-Integrated Circuit) with CoW (Chip on Wafer) and WoW (Wafer-on Wafer). This recently became a push from the need to disintegrate (de-integrate and break down a large chip into smaller parts) of large monolithic SoC (System-on-Chip) manufactured with latest wafer fab technology nodes such as 14 nm and below driven by the digital design into so called Chiplets/Dielets. Those are integrated functional circuit blocks, often reusable IP blocks, that have been specifically designed to work with other similar Chiplets to form larger more complex chips inside a SiP. They have been "invented" in the process of disintegration of SoC into many smaller chips for the following two main reasons:

- Process technologies continued to enable higher monolithic integration in one chip, but SoC sizes reached reticle limits, which dictated the maximum size of chip.
- Economics has resulted in a reversal of that trend due to defect density on large chips directly impacting yield and cost (Figure 4) and significant increased cost for new technology nodes.

Advanced Packaging got the task to enable the rebuilding of the large SoC out of those Chiplets/Dielets targeting the performance of the monolithic SoC or even better, as the functional blocks put together here are manufactured with function optimized wafer fab technologies in different companies with different capabilities, IP ownership, and consequently function specific optimized

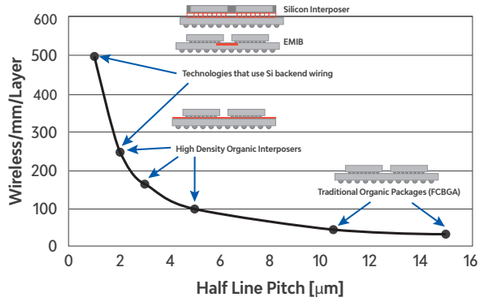
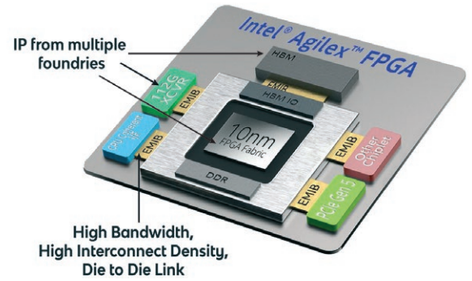


Figure 5: Interconnect density envelopes for different advanced package architectures (Source: Intel).

Figure 6: The Intel Agilex FPGA provides a good example of heterogeneous integration in SiP (Source: Intel).



performance. Customers can do a "Cherry Picking" to build their own "SoCs" out of the Chiplets they consider the best for their applications. However, there is still a lot of work to do such as standardization of interfaces, and development of smallest und shortest possible interconnection technologies between the Chiplets in the package, often thousands of contacts on a few square millimeters.

Given the trends summarized above and the growth in Advanced Packaging shown, the equipment supply chain will be under enormous pressure to support the technology development with tailored equipment and process solutions and to meet capacity and productivity requirements once the industry moves into high volume manufacturing.

A key piece of technology is thin film deposition, both on wafer and panel level up to 600mm square substrates.

Thin film deposition is required to manufacture either seed layers or passivation layers with high uniformity, superior adhesion, lowest resistance and low particle count. Innovative, flexible, high throughput, highly automated and high quality solutions are required by the packaging industry, which in this field are not only OSATs and IDMs anymore, but also Foundries as explained above. Last but not least, physical vapor deposition technology will make it into the Printed Circuit Board (PCB)/ IC-Substrate industry too, as technology leaders move towards smaller feature sizes too, competing with mainly the traditional Fan-out WLP/PLP players. Embedded trace and molded interconnect substrates e.g. using Ajinomoto build-up films (ABF) are on the rise and present new opportunities for thin film deposition technology leaders like Evatec.

About the author

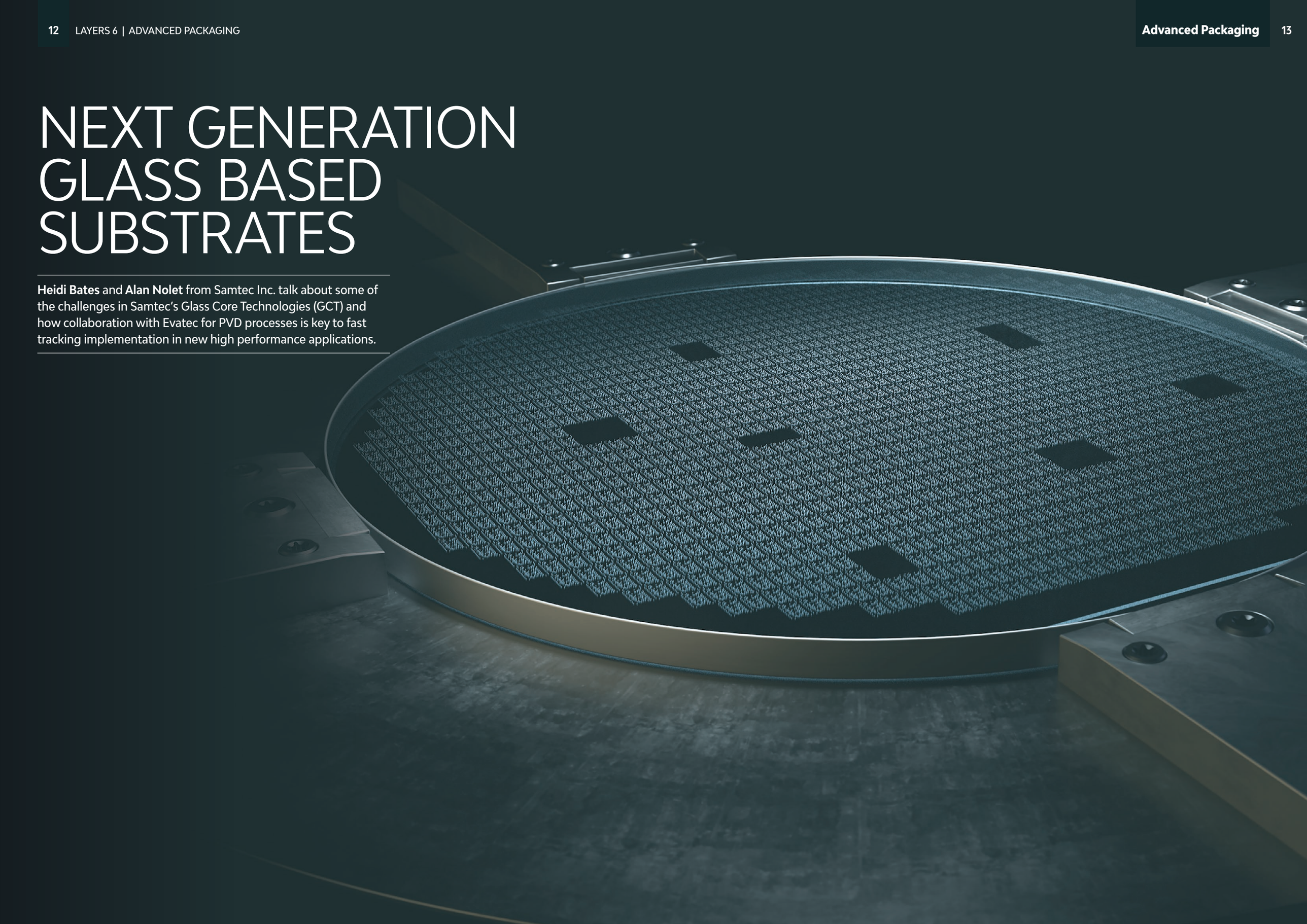
Steffen Kroehnert is President & Founder of ESPAT-Consulting based in Dresden, Germany. He provides a wide range of consulting services around Semiconductor Packaging, Assembly and Test, mainly for customers in Europe. By June 2019, he had worked for more than 20 years in different R&D, engineering and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors, Infineon Technologies, Qimonda, NANIUM and Amkor Technology, where he most recently served as Senior Director Technology Development. Since 2016 Steffen has chaired the European SEMI integrated Packaging, Assembly and Test - Technology Community (ESiPAT-TC).

Steffen has authored or co-authored 23 patent filings and many technical papers in the field of Packaging Technology. He also co-edited the book "Advances in Embedded and Fan-out Wafer Level Packaging Technologies". He is an active member of several technical and conference committees of IEEE EPS, IMAPS and SEMI Europe. Steffen holds a M.Sc. in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

Data and materials for all figures in this article have been kindly provided by the author.

NEXT GENERATION GLASS BASED SUBSTRATES

Heidi Bates and **Alan Nolet** from Samtec Inc. talk about some of the challenges in Samtec's Glass Core Technologies (GCT) and how collaboration with Evatec for PVD processes is key to fast tracking implementation in new high performance applications.



From 5G and sensing to diagnostics and medical implantable devices, modern electronics are getting smaller, denser and faster. Moore's Law has revolutionized the semiconductor process, but it is quickly reaching its practical limits. Systems architects and design engineers must consider all aspects of device engineering.

Additionally, the electronics device industry is evolving to support quicker innovation cycles. From a development viewpoint, emerging solutions must support shorter delivery times, more flexible processes and rapid customization. Advances in materials science also hold the key. New substrate materials and new thin film technology open new doors to ever shrinking, next generation electronic devices.

Emerging glass based substrates

One solution showing promising results is glass-based substrates. They offer high structural integrity, resistance to vibration and temperature, environmental ruggedness and low electrical loss. These properties contribute to faster speeds, small signal-to-signal spacing and ease of use making them ideal for next generation electronics device design.

Fused silica is one example of a material offering huge potential for high performance applications. This substrate choice offers consistent and well matched material characteristics. Although other glass types may be less expensive, a polished synthetic fused silica product of high quality provides low risk of breakage, excellent via drill results, and valued electrical properties which offset the minor cost penalty. It also allows excellent adhesion for the typical subsequent metallization process required.

Via fill and metallization processes are the start

There are several key properties to be achieved for via filling including very low ohmic resistance for high conductivity throughout the signal path and the mechanical, chemical and electrical stabilities essential for satisfying environment stress cycles. Manufacturing processes must also be suitable to achieve the potentially high aspect ratios (e.g. up to 15:1) required over a wide range of via dimensions (20µm – 150µm).

Redistribution layers add to the challenge

Progress does not come without challenges however. While drilling and filling TGVs are just the start of the advanced packaging process, the next challenge is reliable integration of redistribution layers (RDL) onto the top and bottom layers of the glass substrate and to the TGVs. Here again however, the choice of fused silica with its good consistent adhesion properties offers a good base for achieving "excellent" low contact resistance values.

Working with Evatec helped Samtec develop the optimum RDL process for such glass substrates demonstrating key properties like strong adhesion between the metal and glass substrate, a continuous uniform RDL, a high-conductive signal path from top layer through the via to a bottom layer and compatibility from one layer to the next. A cross section in figure 1 shows multilayer deposition on filled vias in a synthetic fused silica glass.

Evatec and Samtec specialists worked side-by-side in the ECL.

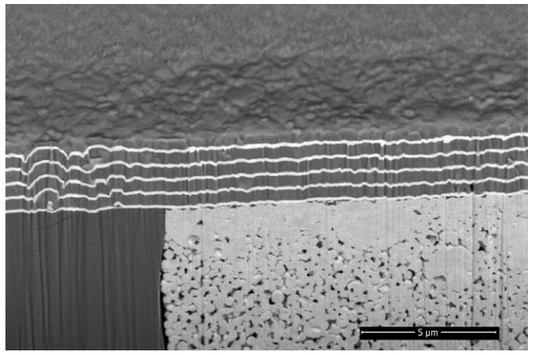


Figure 1: Advanced SEM technology illustrates the success of this collaborative approach. The Samtec/Evatec process demonstrates multiple layers of "interrupted" barrier/conductor depositions on SAMTEC XFilled vias in AGC Synthetic Fused Silica Glass.

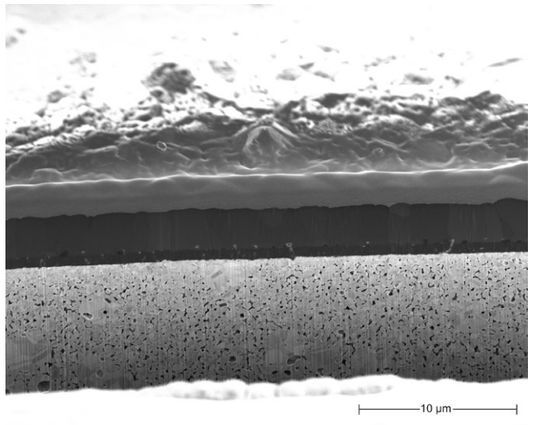


Figure 2: shows how layer functionality can be combined in successful deposition of a film fulfilling three functions of adhesion, barrier and conductor deposition on synthetic fused silica using technologies like highly ionized sputtering (HIS).

Collaboration is key for success

Evatec leveraged the CLUSTERLINE® 200 capabilities in its dedicated ECL development cleanrooms to support Samtec in TGV and surface metallization PVD processing techniques adapting the system to handle 150mm wafers. The Evatec specialists worked side-by-side with the Samtec GCT team in several rounds of process development to achieve the encouraging results to date.

Now that our teams have completed the proof-of-concept phase by developing processes successfully marrying fused glass substrates, we can optimize and expand capabilities for unique customer applications while evaluating additional processing techniques.

About Samtec

Samtec's Glass Core Technology (GCT) group develops processes that leverage performance benefits of glass enabling optimized, miniaturized substrates. Samtec also utilizes glass substrates in interposers. Passive interposers combine substrates, through-glass via (TGVs) and unique via metallization capabilities. Active interposers add additional functionality with circuit patterning and discrete component capabilities.

Samtec's GCT technical experts have developed three production-grade TGV filling processes. Each offers unique characteristics ideally suited for specific markets. One takes advantage of electro-chemical deposition (ECD) for fill plating the TGVs. A second uses a thick film paste that combines a conductive metal choice and additives for performance customization. The third, XFil, features pure metal micro particles simply stored as a suspension and efficiently filled directly in the vias.

Samtec's unique XFil technology provides differentiation compared to plating and thick film paste via fill solutions. The foundation of XFil technology is the use of pure metal micro/nano powders. No additives, fillers or residuals are required. Since the resultant via fill material is pure metal, the electrical and mechanical properties are optimized and easily adjusted. The choice of metal powder is flexible and simply customized to the end application.

From a process standpoint, XFil offers additional benefits. It is substrate and form factor agnostic. The XFil via filling process works well with coupons, wafers and eventually panels. XFil saves material cost with minimal waste and extremely long shelf life. The via filling equipment is simple, with minimal process control requirements and excellent co-planarity results.

Over the past several years, Samtec has developed significant internal capabilities for glass drilling, via filling and RDL deposition and patterning. Additionally, Samtec offers a complete suite of metrology and electrical testing capabilities for substrates and interposers. These capabilities have been crucial in integrating XFil and RDL technology in the package and glass device process.

For more information about Samtec, visit **www.samtec.com/GCT**

All images in this article (except the ECL) have been kindly provided by the author.

Through Glass Vias for glass interposer applications

Kevin Kroehnert and **Markus Woehrmann** from Fraunhofer IZM introduce the merits of Through Glass Via (TGV) technology and factors to consider in optimizing its processing route in comparison with more established Through Silicon Via (TSV) technology.

Introduction

Although TSV technology is well established in the semiconductor industry for 2.5D and 3D applications the properties of silicon limit its use in some applications. The application of TSVs is only realized in products in high price segments, like silicon interposers for high end GPUs or FPGAs. Glass interposers and through glass vias (TGVs) are becoming more and more attractive as an alternative for 3D packages instead of silicon based interposers. This is related to the superior performance of glass. It can provide an attractive solution addressing some of the conceptual limitations for next generation packaging designs. Glass offers high optical transparency over a wide range of wavelengths, it has good electrical insulating properties and good chemical resistance and it is well suited for RF applications due to its low loss tangent and permittivity [1]. It can be tailored for different applications by modification of its composition and a wide variety of glass materials are commercially available today from different material suppliers. The thermal coefficient of glass can be matched to silicon which makes it a good material to implement active devices into or on glass interposers [2] [3]. For hermetically sealing of a device and also realizing an electrical contact to the inner circuitry, TGVs can be used as vertical interconnects to feed the signal in and out of the packages. And last, but not least, the TGV generation in glass instead of TSV generation in silicon shows cost benefits regarding the different process flow.

TGV Formation

TGVs can be created by different methods. Glass suppliers have offered TGVs and already metallized TGVs in their product portfolio since some time, but today the choice of processing technologies for initial TGV formation is wider than ever. Former and current methods include Laser Induced Deep Etching (LIDE®), Laser Ablation, Sandblasting, UV Exposure, Electrical Discharge (AGC), US Drilling and Over Moulding (Hermes). (Note: The TGVs metallized in the work presented below were produced predominantly by LPKF using Laser Induced Deep Etching (LIDE) technology."

In the past 6 years glass and tool suppliers have improved the glass via formation process, which has lead to tremendous increases in the aspect ratios possible for TGVs and demonstrated feasibility for mass production. Companies, like LPKF now offer foundry services for glass substrates with vias as part of a new supply chain for glass interposer devices.

The different via generation techniques in combination with the large variety of via diameter and aspect ratios required by the broader application field set new challenges for the processes flows which follow. Together with our partners, Fraunhofer IZM Berlin has developed such process flows including "temporary carrier" based flows for glass substrates with thickness below 300 µm, or cost effective "carrier less" flows for thicker substrates. All the processes are based on the wafer level line for RDL and TSV processing, which guarantee a simple transfer of the flow into mass production. Fraunhofer IZM has successfully metallized vias in glass with a diameter ranging from 10µm to 1mm at thicknesses of the glass interposer from 40µm to 470µm.

An overview of some of TGVs which were metallized at IZM can be seen in figure 1.

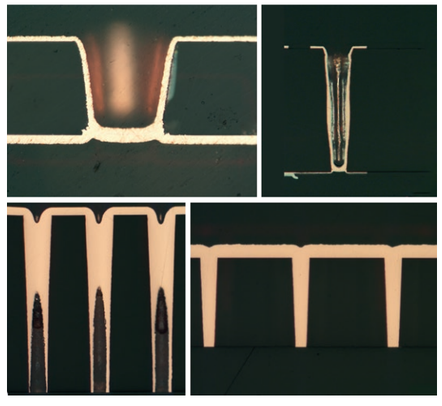
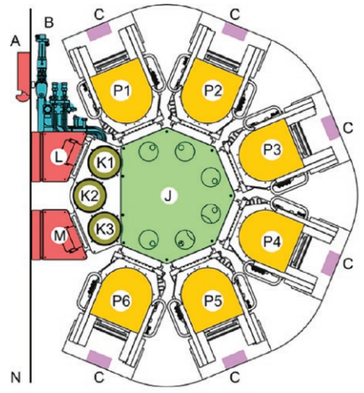


Figure 1: Via Geometries: Clockwise: Depth: 40µm Dia:30µm, Depth:100µm Dia:20µm (Vias created with LIDE), Depth:300µm Dia: 50µmm Depth 470µm Dia;80µm (Vias created by LIDE).

TGV Metallization

For metallization of the glass interposer we use an Evatec CLUSTERLINE® 200 with a fully equipped transport module. This fully automated single wafer processing tool is configured for 200mm or 150mm wafers as shown in figure 2. It comprises two automatic load locks for 25 wafers (6" and 8"), a transfer module included two-arm robot, a pre-aligner station. For TSV and TGV applications the system has been equipped with an ICP sputter module for substrate pre-treatment and two HIPIMS (High Power Impulse Magnetron Sputtering) stations for Titanium and Copper film deposition. The system also integrates degas and cooling modules.

Figure 2: Evatec's CLUSTERLINE® 200 II system overview.



The CLUSTERLINE® 200 and its HIPIMS process modules enable metallization of TGVs and other features with high aspect ratios. We are able to process glass wafers with through holes or blind holes (known from TSV interposers) with different via shapes (due to different fabrications methods used for via formation) according to different requirements. Of course the process which is normally used for silicon interposers had to be modified significantly due to the different properties of glass wafers. The main differences to silicon interposers which have to be considered for the sputtering process are summarized in table 1.

Adhesion and seed layers have to be formed in the via of the glass interposers which are thick enough to allow electroplating. Two PVD modules dedicated for HIPIMS deposition are optimized for this process, one for the titanium adhesion layer and one for the copper seed layer. HIPIMS is a pulsed DC process that uses very short power pulses with low duty cycles and very high peak current of several hundred amperes. Very high plasma densities can be achieved using this technique [4]. By applying an RF-bias voltage on the substrate the ionized metal is accelerated across the sheath to the substrate in a very narrow angular distribution and deposits a continuous film [4] both within the vias and on top of the wafer as illustrated in figure 3.

Glass Property	Comment
Thermal conductivity	Lower than silicon. Heat can therefore not be transferred to the cooled chuck as fast as silicon.
Via geometry	The via shape varies depending on the via formation technology and is normally not comparable to a via in silicon which is created by a BOSCH process.
Via size	With a thicker interposer and bigger diameter of the via, the surface area which has to be covered in the via is greatly increased.

Table 1: Major differences between TSVs and TGVs.

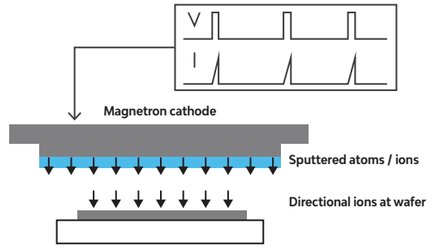


Figure 3: Evatec HiPIMS schematic principle.

As already discussed, the sputtering process has been adapted to address the major differences between the typical silicon and glass interposer The heat which is generated during sputtering is normally transferred through a cooled chuck to keep the wafer temperature in the acceptable process window. To compensate for the lower thermal conductivity of glass, the pauses between deposition cycles have to be extended in duration which increases the whole process time. To cater for different via shapes and via sizes more

material must also be deposited. For TGVs which go through the whole wafer it is also an option to sputter the wafer from both sides.

Electroplating is performed after sputter deposition. Depending on application and via geometry we are able to provide the via liner plated, hermetically plated or fully filled with copper.

Figure 4 illustrates two TGV examples. In the first one the liner is plated and in the second it has a copper plug on the top side to close the via for use in an application where hermetic sealing is necessary.

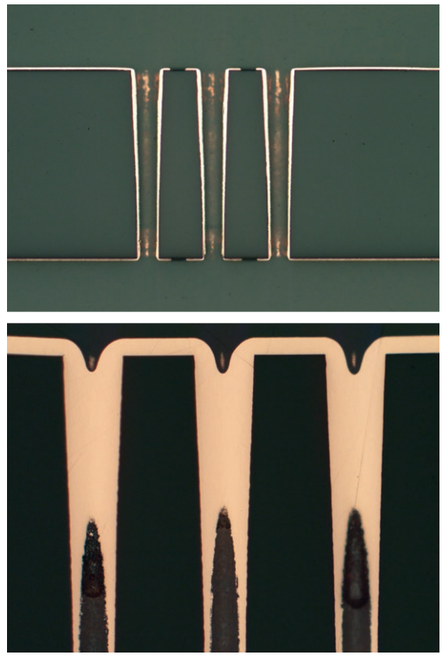


Figure 4: Top: 470µm interposer with 80µm via and plated copper liner; bottom: same via with copper plug (Vias created with LIDE).

After electroplating a thick layer of copper normally covers the whole surface of the wafer. This so called "overburden" is typically removed by consecutive wet etching and a CMP (chemical mechanical polishing) process and leads to a revealed copper liner on both the frontside and backside of the wafer. In figure 5 the wafer surface after the final CMP process of a liner plated TGV shows a small revealed copper ring around the perimeter of the via, making it suitable for further contacting with a redistribution layer.

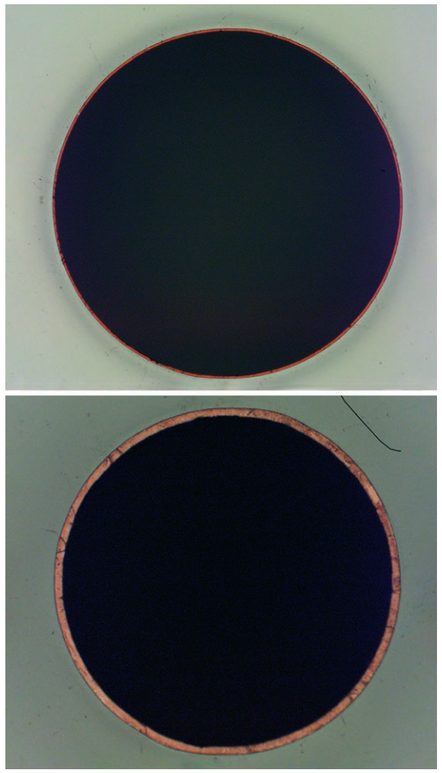


Figure 5: TGVs after CMP; top 80µm diameter, bottom 300µm.

After revealing the TGVs, the wafer can be further processed from the bottom and top side depending on requirements of the finished products.

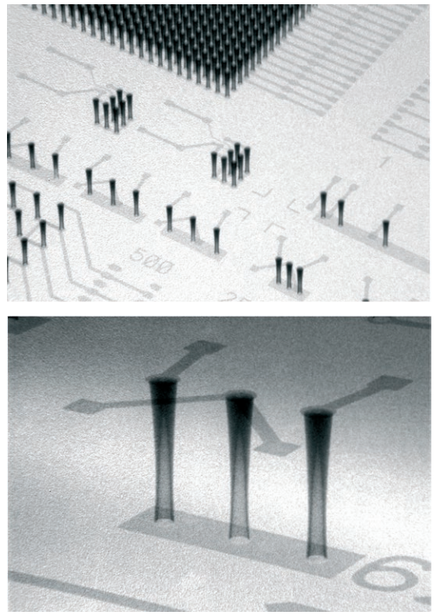
For electric testing and characterizations of TGVs, a wide spectrum of analyses can be carried out. Typical characterization methods include reliability testing (daisy chain structures), DC measurements (Kelvin structures) and RF measurements (Figure 6).

Reliability data of daisy chain structures and final interposer packages shows that thermal cycling with more than 1000 cycles (-55°C/+125°C) does not affect the TGV performance.

Application example

The GLARA project financed by the German Ministry of education and Research (BMBF) is just one example of projects undertaken by Fraunhofer IZM and illustrates an application for of TGVs. The project involved fabrication of a hermetically sealed glass package containing a 160GHz radar ASIC from Endress and Hauser for distance

Figure 6: Kelvin and daisy chain structures in a glass interposer for electrical characterization and reliability testing.



ranging of level sensors. The ASIC is normally connected with via bonds and is mounted on a microwave PCB. The hermetic packaging of the device reduced packaging costs, decreased parasitic losses due to the missing bonding wires and shorter interconnects and sealed the ASIC inside. The package used two glass interposers to make use of the superior RF performance of glass compared to silicon. The bottom interposer was 470µm thick and contained a cavity to house the ASIC. The upper glass interposer (100µm thick) was used to mount the ASIC and to connect its antenna and the bonding pads. The thicker bottom interposer had balls on its underside to assemble it on a PCB. The whole process was done on wafer level using 200mm B33 glass wafers. The TGVs in the bottom interposer (fabricated with LIDE) had a diameter of 80µm and the TGVs in the top interposer had a diameter of 20µm.

Project partners were Endress & Hauser, Pactech Gmbh, LPKF AG, University Ulm, Sentronics Metrology GmbH, and MSG Lithoglas GmbH.

Want to know more?

If you would like to know more about TGV processing and capabilities at Fraunhofer IZM please don't hesitate to contact the authors via kevin.kroehnert@izm.fraunhofer.de

Acknowledgment

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Data and materials for all figures in this article (except 2 & 3) have been kindly provided by the author.

SCALING TO FINE FEATURES FOR CHIPLETS ON LARGE PANELS

Tim Olson, Founder & CEO of Deca and Evatec's **Roland Rettenmeier,** Senior Product Marketing Manager, Business Unit Advanced Packaging, explain the history, development and benefits of M-Series™ and Adaptive patterning and how roll out of volume manufacturing by industry leaders including Nepes and ASE demonstrates that the technology has a bright future.

Deca was born out of a passion to transform the way the world builds advanced electronic devices. In our first decade, our 10X thinking brought to life exciting breakthroughs including M-Series™ fan-out wafer level packaging (FO-WLP) and Adaptive Patterning™. Through divestiture of manufacturing operations in 2020, Deca became a pure-play technology and licensing company.

From the earliest days, the influence of SunPower's large format solar wafer manufacturing process underpinned Deca's vision of creating the highest levels of electronic interconnect technology on a large panel format. FO-WLP provided the physical realization through M-Series and Adaptive Patterning, now shipping in high volume and found in the world's leading Smartphones facilitated by emerging industry standards. The strong market growth figures expected for the FO Panel market up until 2023 are illustrated in figure 1.

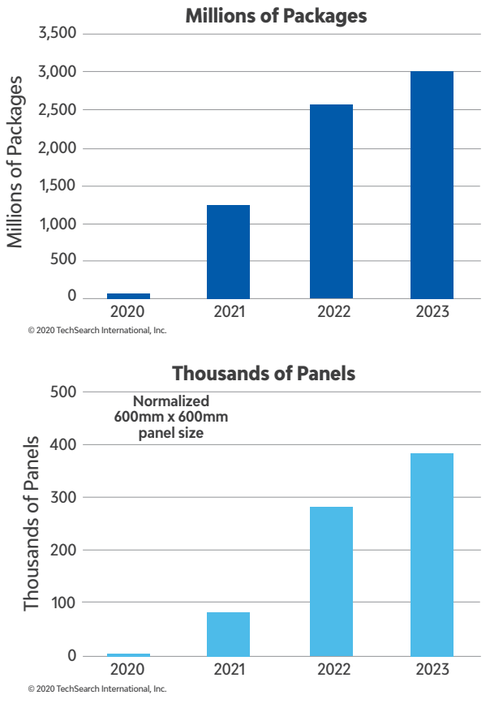


Figure 1: Forecast for low-density FO Panel Demand. Courtesy of Tech Search.

Multiple industry analyst reports, including the i-micronews article published in July 2019[1] have outlined the quality and reliability benefits of M-Series which sets the technology apart from industry competitors. M-Series is a chips-up fan-out technology. Cross-sectional views of chips-down fan-out (eWLB) and TSMC's chips-up fan-out (InFO) are shown in figures 2 and 4 respectively with M-Series in figure 3.

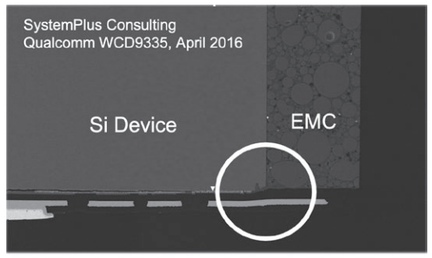


Figure 2: eWLB.

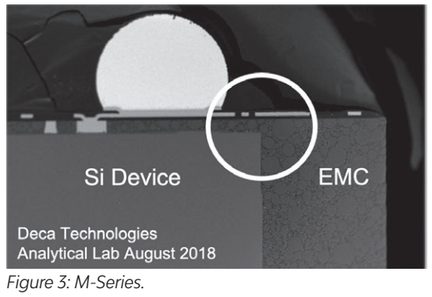


Figure 3: M-Series.

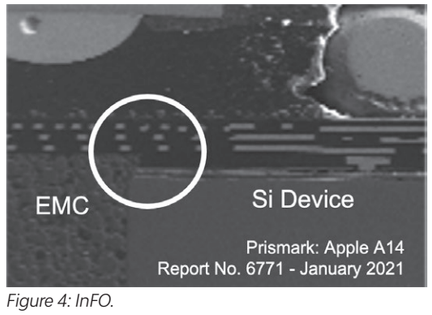


Figure 4: InFO.

Conventional fan-out is manufactured in a face-down process flow with the active face of the semiconductor device left exposed after the molding step. As encircled in figure 2, there is a discontinuity between the device surface and the electronic molding compound (EMC) leading to multiple process limitations as well as quality and reliability concerns. As highlighted in figure 3, the M-Series structure embeds the sensitive active semiconductor region of the device within EMC while providing a planar surface to alleviate process concerns in subsequent fab build-up layer processing. The embedded nature of M-Series with the EMC buffer layer over the device has been proven to significantly extend BLR (board level reliability) as compared to conventional WLCSP (wafer level chip-scale packaging) and eWLB which rely only on a polyimide (PI) or polybenzoxazole (PBO) material over the semiconductor device. While not easily discernable, the InFO structure shown in figure 4 similarly provides a planar surface for fab build-up layer processing, however, still relies on PI or PBO as the only protective material between the device and the electronic appliance printed circuit board (PCB).

Deca has established technology and license agreements with ASE Group (Advanced Semiconductor Engineering Inc.), the world's largest outsourced semiconductor assembly and test company (OSAT), and Nepes Corporation, a leading-edge provider of wafer and panel-level packaging foundry turnkey solutions. M-Series is currently produced in volumes measured in millions per day on 300mm wafer formats with plans in progress for full 600mm implementations at both Nepes and ASE to support robust demand growth. Multiple other manufacturing service providers including wafer foundries, substrate producers, and OSATs are in technology and licensing discussions or under consideration for expansion of the global M-Series and Adaptive Patterning production footprint.

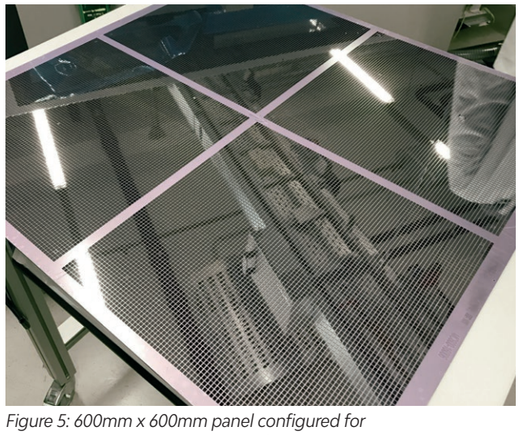


Figure 5: 600mm x 600mm panel configured for quartering to 300mm square panels.

Deca established the new 600mm x 600mm large panel manufacturing format for M-Series in 2010 with considerations for both short-term implementation and long-term optimized productivity.

The ability to segment the 600mm format into four equal 300mm square sub-panels as illustrated in figure 5 for use with conventional 300mm round wafer probe test equipment was a key short term consideration. 300mm square segments also provided achievable initial process extension targets for uniformity on critical processes including metal deposition, thin film coating and direct-write lithography while keeping in mind the ultimate utilization goal of the entire 600mm panel area. Seed layer deposition is one of the most critical process steps in manufacturing vertical and horizontal interconnects and has a direct impact on the overall package reliability and performance.

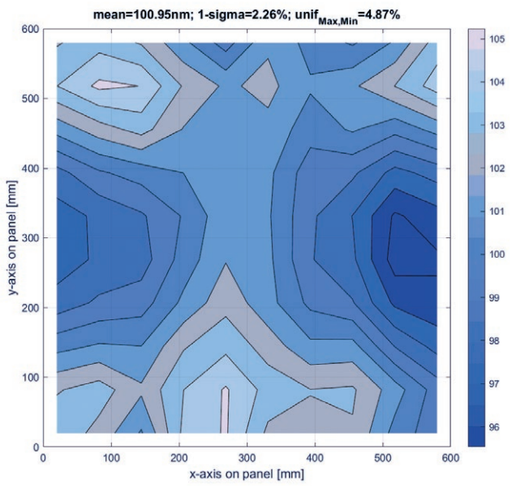


Figure 6a / 6b: Deposition uniformities on 600mm panels processed on CLUSTERLINE® 600 courtesy of Evatec.

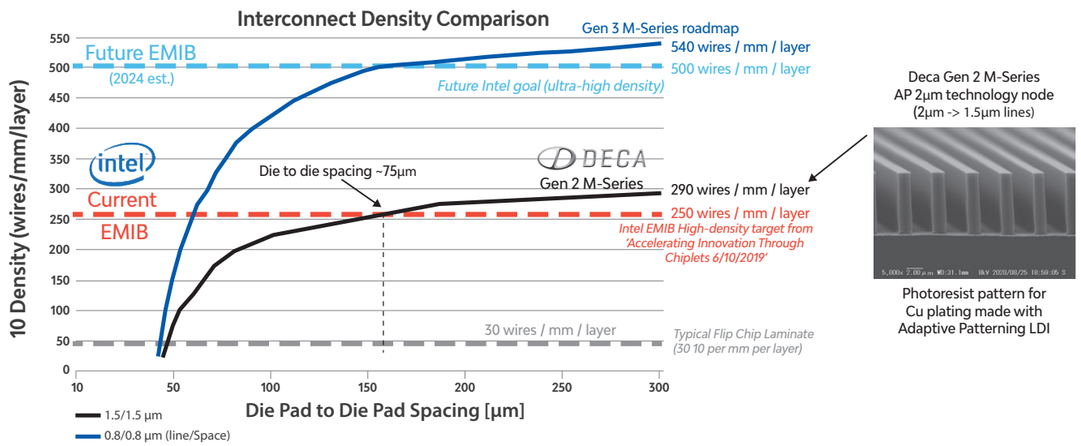
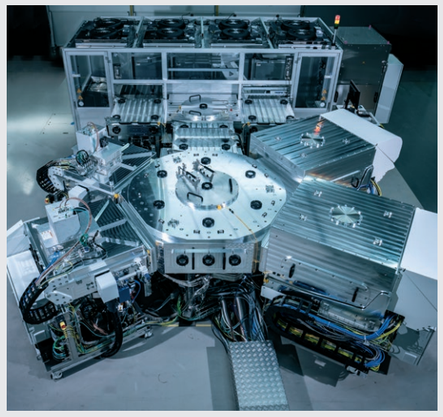


Figure 7: Wiring density comparison of EMIB vs. Gen 2 M-Series.

Successful 600mm panel processing calls for high performance degas, etch and sputter deposition processes across the full substrate area, plus well managed substrate temperature throughout the whole process to ensure low contact resistance (Rc) and excellent adhesion of the deposited seed layers prior to downstream electroplating and lithography processes. Figures 6a and 6b show that deposition uniformities for Ti and Cu layers deposited on commercially available production tools like Evatec's CLUSTERLINE® 600 now fall well within required specifcations.

In scaling up to the 600mm format, provisions for scaling down to 2µm line and space have also been included. One of the most critical capabilities supporting the simultaneous scaling up in panel size and down in feature size is Adaptive Patterning which introduces real-time design during manufacturing to accommodate natural process variation. Adaptive Patterning includes Deca's proprietary AP Studio EDA tool where designers create rules and boundaries within a new product design that are executed upon for each device in every wafer (or panel) within AP Engine performing real-time design during manufacturing. Through mask-less laser direct imaging (LDI), a unique design file for every device is utilized to align, re-route or re-shape any or all dielectric and metal build-up layers in real-time to ensure precise creation of the as-built semiconductor interconnect. With the latest 2µm line and space capability, benchmark high-density interconnect of over 200 wires/mm/layer can be achieved together with 20µm area array bond pad pitch. For heterogeneous integration of chiplets, these capabilities provide competitive, and in some cases, superior, capability to industry leading solutions including Intel's EMIB (embedded multi-die interconnect bridge) and TSMC's InFO (integrated fan-out).

Deca's Gen 2 M-Series and Adaptive Patterning technology achieve equivalent wiring density as compared with Intel's EMIB as shown in figure 7.



CLUSTERLINE® 600

"Evatec's CLUSTERLINE® 600 is qualified at major OSAT and IC-Substrate maker for superior degassing, etching and seed layer deposition - one important piece of the whole puzzle.

We are looking forward to see Deca's technology lift off and boost FOWLP and FOPLP to the next level. Smaller L/S geometries and smaller pads sizes for more precise vertical interconnects and more space for routing offer big potential to the packaging industry."

Roland Rettenmeier,
Evatec

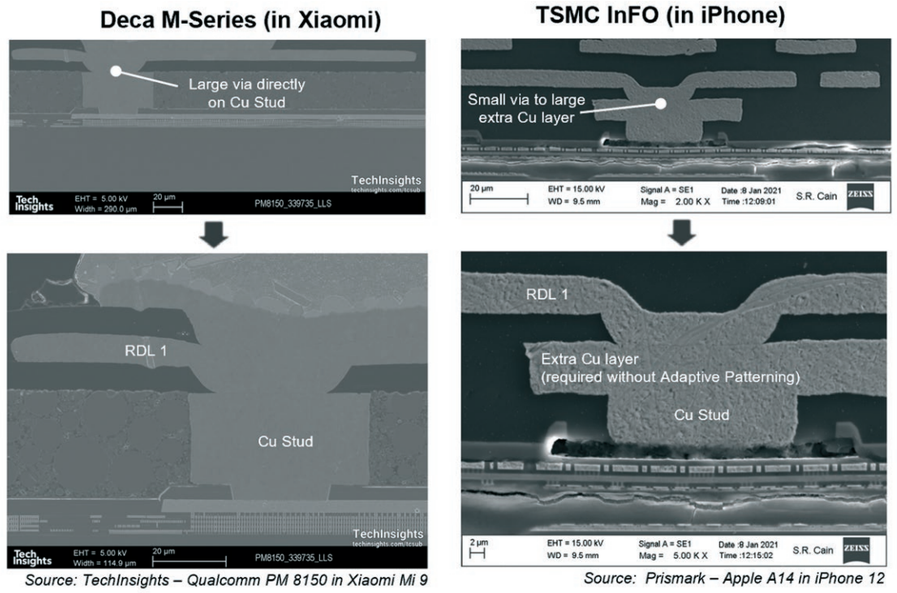


Figure 8: Device bond pad interface critical dimension comparison.

Source: TechInsights – Qualcomm PM 8150 in Xiaomi Mi 9

Source: Prismark – Apple A14 in iPhone 12

M-Series achieves equivalent density to the bridge chip structure within a simple planar fan-out RDL build-up eliminating the cost and complexity of embedding silicon bridge chips within a substrate.

Through the use of Adaptive Patterning, M-Series provides the capability to scale bond pad pitches to ever finer levels. Generation 1 provides the ability to scale to 45 µm area array bond pad pitch with a robust 15 µm polymer via precisely alignment to a 30µm Cu stud while Gen 2 supports a breakthrough 20µm array bond pad pitch using a 6µm polymer via precisely aligning to a 12 µm Cu stud, In comparison, TSMC's latest InFO is restricted to broader bond pad pitches with an oversized 50µm extra Cu layer added above the Cu stud to compensate for the lack of Adaptive Patterning. Third party teardown analyses showing Deca's Gen 1 M-Series vs. TSMC's latest InFO found in the Apple iPhone 12 is shown in figure 8.

For this specific power management device, a larger 50 µm Cu stud was chosen by the customer along with a 30 µm via connection made through Adaptive Patterning directly to the Cu stud without the need for an extra Cu layer.

In summary, as the semiconductor industry transitions away from monolithic silicon scaling in favor of heterogeneous integration and chiplets, fan-out technology is increasingly becoming the preferred choice of IC designers and system architects. Deca's M-Series fan-out with Adaptive Patterning is positioned to grow from its current Gen 1 leadership position in single die applications to the plan of record for ultra-high-density chiplet integration with Gen 2. With ASE's and Nepes' four combined manufacturing facilities in three countries in production or preparing for qualification along with multiple other potential licensees coming soon, scaling to fine features for chiplets on large panels with M-Series and Adaptive Patterning is on a well-defined path to success.

For more information visit **www.thinkdeca.com**

DECA
www.ThinkDeca.com

Ref 1: https://www.i-micronews.com/new-commercialization-of-deca-technologies-fan-out-technology

Data and materials for all figures in this article (except 1 & 6) have been kindly provided by the author.

THANK YOU FOR READING

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We hope you have enjoyed reading this edition of LAYERS. We welcome your feedback about our magazine and ideas for topics that you would like to see addressed in future editions.

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