# CHIPLETS AND THE NEW ERA OF ADVANCED PACKAGING

***E. Jan Vardaman*, President and Founder, TechSearch International Inc. reviews the state of play and the challenges ahead.**

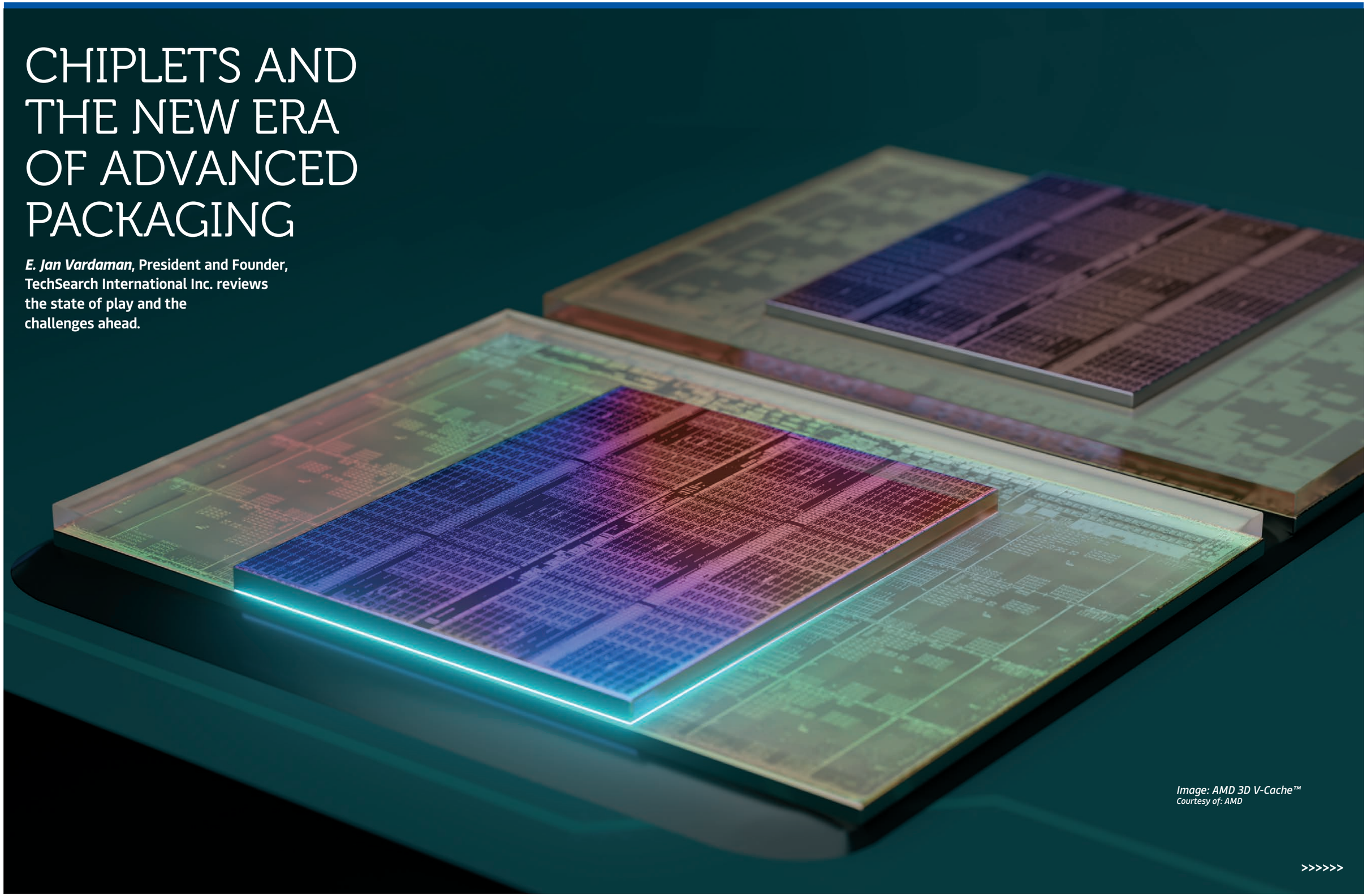

*Image: AMD 3D V-Cache™*
*Courtesy of: AMD*

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As the industry enters the new era of heterogeneous integration, advanced packaging in the form of chiplets is becoming increasingly important. An increasing number of companies are turning to chiplets to achieve the economic advantages lost with expensive monolithic scaling, ushering in a new era of smart packaging. A chiplet is not a package, but it is a new approach to system, package, and chip design. There are many package options that can be adopted and careful consideration is required to select the most appropriate options for the application. Options include the emerging 3DIC format with mircobumps or hybrid bonding, laminate substrate package, fan-out on substrate, and silicon interposer. Challenges include design, test, assembly and thermal management.

## What is a Chiplet and what are the advantages?

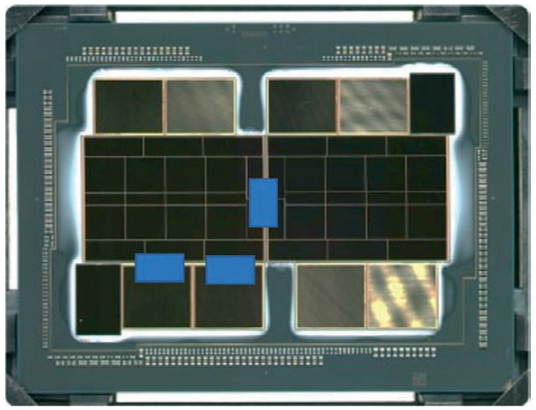
A chiplet is a functional circuit block and includes reusable IP blocks. A chiplet is a physically realized and tested IP with a standard or proprietary communication interface between IP blocks. A chiplet functions with other chiplets, so the design must be co-optimized and the silicon cannot be designed in isolation.

There are numerous advantages with the use of chiplets. AMD indicates that the major drivers for its adoption of chiplets include rising manufacturing cost for large die, increased cost of mask sets, increased complexity of design rules in leading-edge nodes, and architectural challenges of meeting relentless demand for increased computational power. It is also possible to have higher core counts and therefore higher performance than with a monolithic design.  Cost savings at the die fabrication level can be obtained by partitioning die and only fabricating the logic functions on the most advanced nodes where needed most. Smaller die also result in higher yield per wafer, resulting in cost savings. Binning the chiplets provides an opportunity to optimize performance even further. There is a trade-off of increased cost at the packaging and assembly level. Additional costs with chiplets include increased area for interfaces, a more complex design, and often a more expensive package. However, the benefits outweigh the costs.

One of the greatest challenges is how to connect chiplet IP blocks to communicate with each other. There are many different interface options for chiplet communication. There is no single standard die-to-die interface solution in the market today. Many are proprietary, but several organizations are developing open standards. The full potential of chiplet design will not be reached until standards are established.

AMD's proprietary interface architecture is called Infinity Fabric (IF). It has been described as a superset of Hypertransport allowing for fast connectivity between different chiplets. The interface connects CPU blocks to each other and can be used to connect GPU blocks. AMD has introduced multiple generations of server and desktop products using chiplet designs [1].



| Attribute | PVC 2T |
|---|---|
| D2D Pitch | 36µm |
| Top Die Count | 20 |
| Max Top Die Size | 41mm² |
| Base Die Size | 650mm² |
| EMIB Pitch | 55µm |
| Core Pitch (min) | 100µm |
| Memory (HBM) | 8x (8Hw/BSM) |
| Package Size | 77.5 x 62.5mm |
| EMIB Count | 11 |

*Source: Intel*


*AMD INSTINCT™ MI200 OAM Series, Courtesy: AMD*

Intel has introduced Foveros technology as a chiplet solution in which a logic die fabricated on an advanced 10nm node is connected to a base die containing I/O and other functions. The base die is fabricated in a less advanced 22nm node. Intel refers to chiplets as tiles. Intel's Embedded Multi-Die Interconnect Bridge (EMIB) was developed so that the high-density connection is placed only where needed, between the die that need to communicate with chiplets such as a logic die, transceivers, and HBM. With EMIB the substrate supplier places a high-density silicon bridge in a laminate substrate. With Intel's new GPU, Foveros tiles and HBM stacks are connected using EMIB. Intel refers to this as co-EMIB [2]. Intel's Ponte Vecchio uses a combination of Foveros and its Embedded Multi-Die Interconnect Bridge (EMIB). Two Foveros 3D configurations are in the center, plus eight HBM stacks, and two additional chips, connected with 11 silicon bridges in the EMIB. Intel will use its modular die fabric (MDF) proprietary interface for its first CPU server for datacenters.

Intel offers its AIB, a die-to-die PHY level standard royalty free. Open Domain-Specific Architecture (ODSA) has introduced Bunch of Wires (BoW). A new standard interface for chiplets, Universal Chip Interface (UCIe) is being proposed by the UCIe Consortium with members including Intel, AMD, TSMC, Microsoft, Meta, Google, Qualcomm, and ARM.

## Chiplet Package Options

A chiplet can be created by partitioning a die into functions and is typically attached to a silicon interposer or organic substrate today, but new options are emerging such as advanced fan-out, RDL interposer, embedded bridges, and 3D stacking. The close cooperation between all segments of the industry, EDA tool vendors, IC designers, third party IP providers, foundries, and OSATs will help drive the growth of chiplets into a wide range of applications.

## Laminate Build-up Substrates

AMD's server, desktop, and gaming products use a laminate build-up substrate with fine features to support their chiplet designs. Intel's Foveros technology with microbump connections between the chiplets (called tiles by Intel) uses a laminate substrate to complete the package.

## Silicon Interposers

Silicon interposer with their ultra high-density connections can support chiplet designs. Xilinx, now part of AMD, continues to use a silicon interposer for its high-end FPGA products that are fabricated in slices. Marvel will introduce a chiplet design for network switch applications using a silicon interposer.

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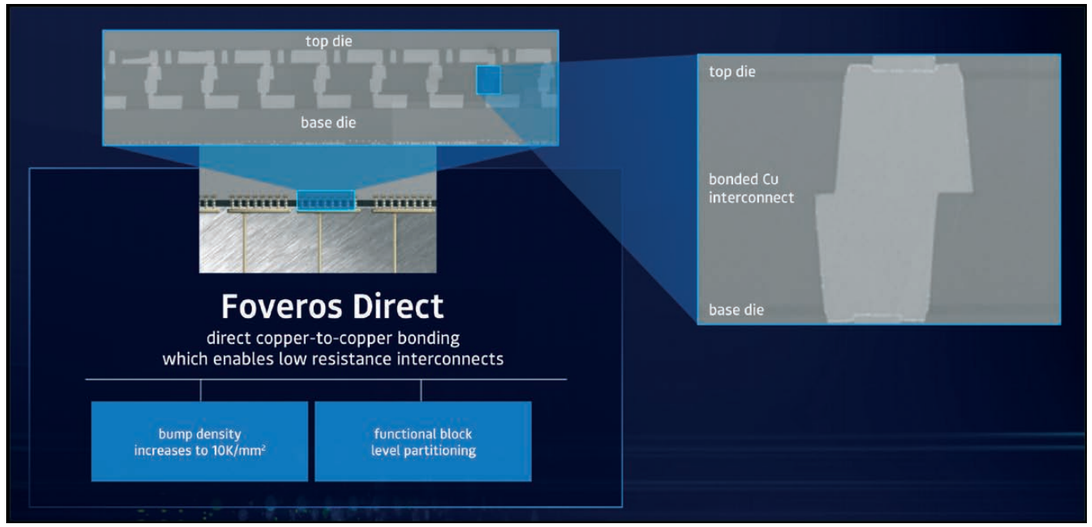


*Source: Intel*

## Fan-out

Companies including ASE, Amkor, JCET, SPIL, Tongfu Microelectronics, and TSMC have introduced fan-out on substrate options for chiplets. TSMC has demonstrated a 51mm x 42mm area with five redistribution layers (RDLs) on a 110mm x 110mm substrate. A 36µm die-to-die I/O pitch has been demonstrated [3].

Companies have also introduced fan-out options with and embedded bridge. The embedded bridge provides the potential for a reduction in the number of RDLs and a more relaxed feature size, resulting in higher yields. AMD's INSTINCT MI200 Series, used for machine learning, is packaged by an OSAT using Elevated Fanout Bridge (EFB) technology. GPU chiplets are connected to the HBM using a silicon bridge embedded in the RDL. The package contains two fan-out modules. Each fan-out module contains one AMD CDNA™2 die (chiplet) and four stacks of HBM2E for a total of 2 CDNA™2 die and 8 HBM2Es. The two fan-out modules are attached to the laminate substrate.

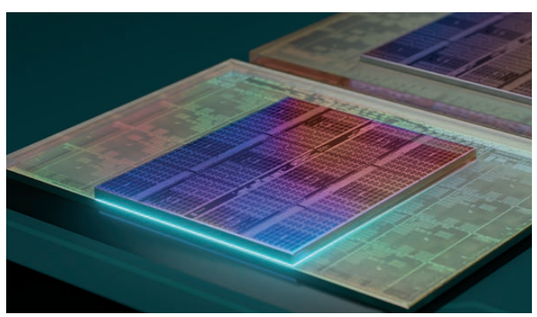

*Image: AMD 3D V-Cache™*
*Source: AMD*

## 3D IC with Hybrid Bonding

TSMC has shown that 3D solutions such as its SoIC™ using hybrid bonding to connect pads without bumps result in higher interconnect bond density. This allows the chip designer flexibility and extensibility on designing a new chip and new system device, adopting the most advanced integration technology for cost and performance advantages. Electrical resistance is lower because there is no solder bump. Lower insertion loss is also reported. High-quality signal integrity and power integrity with low RC delay and low IR drop are also reported. Energy consumption/bit is lower (as measured in pJ/bit) and thermal resistance is lower. This means less energy is required to move data around. With a fixed power envelope, less energy spent per bit means that more bits can be transferred or that the saved energy can be spent on other resources. AMD V-Cache™ using TSMC's SoIC™ technology is in production for server, desktop, and gaming products. A laminate substrate is used for the package. TSMC explained the advantages of a 3D structure with hybrid bonding over a side-by-side chip layout on a silicon interposer or 3D stacking with microbumps for its SoIC™ process (see table page 23).

## Intel's Foveros Direct

Intel is developing a 3D hybrid bonding process for its Foveros technology. The focus is on sub-10µm pad pitch. In the development of its hybrid bonding process, Intel notes that there are new requirements on the bonding layer, die properties such as flatness, and tolerance to process temperatures. Design considerations include the need to consider the impact of top layer passives such as high-speed signal routes, inductors, and transforms due to increased coupling of the die (due to the proximity of the die surfaces).

**SoIC™ Compared to 2.5D and Conventional 3D IC**

| | 2.5D | Conventional 3D IC | SoIC |
|---|---|---|---|
| Interconnect | µbump + BEOL | µbump | Bumpless |
| Chip distance | 100 µm | 30 µm | 0 |
| Bond pad pitch | 36 µm (1.0X) | 36 µm (1.0X) | 9 µm (0.25X) |
| Speed | 0.01X | 1.0X | 11.9X |
| Bandwidth density | 0.01X | 1.0X | 191.0X |
| Power dissipation | 22.9 | 1.0X | 0.05X |

*Source: TSMC*

IBM Research is working to develop hybrid bonding for future products. 3D chiplets will be stacked using nanosheet logic die stacking. Nanosheet refers to the silicon generation that follows FinFET. The 3D stack will be mounted on a high-density laminate substrate. Samsung Electronics is developing a 3D hybrid bonding process. The focus is on logic such as CPU, GPU, and NPU plus SRAM (cache memory).

While hybrid bonding offers many advantages, there are also challenges. Samsung is focused on addressing challenges such as Cu pad surface control, cleanliness, pad alignment accuracy, bonding temperature, metrology, and developing an integrated bonding/assembly system [4].

## Promises and Challenges

There are tremendous advantages with the adoption of chiplets, especially using 3D hybrid bonding. 3D hybrid bonding will also offer much greater advantages than could ever be reached with monolithic scaling. The adoption of chiplets will have a similar impact on the industry as the move from peripheral chip layout to area array. The chiplet strategy is not without its challenges and associated cost. Packaging chiplets is expensive. Co-design is a must. Chiplet IP blocks must be able to communicate with each other. Standard interfaces are needed. Careful thermal analysis is important, especially with 3D stacking. Hybrid/bumpless bonding requires a clean surface for bonding and a clean environment. Particles will result in failures. New test and inspection methods are needed. These challenges are not insurmountable and an increasing number of chiplet solutions are entering the market with a growth rate of 76% expected over the next three years. ◻

**E. Jan Vardaman** is president and founder of TechSearch International Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow. She is a member of MEPTEC, SMTA, and SEMI. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

1. S. Naffziger et al., "Pioneering Chiplet Technology and Design for the AMD EPYC and Ryzen Processor Families," *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture*, June 2021, pp. 57-70.

2. E. J. Vardaman et al., "Quantifying the Impact of Heterogeneous Integration: Chiplets and SiP," TechSearch International, Inc., February 2021.

3. Y. Chiang et al., "InFO_oS (Integrated Fan-Out on Substrate) Technology for Advanced Chiplet Integration," *Virtual Electronic Components and Technology Conference*, June 1 - July 4, 2021, pp. 130-135.

4. S.W. Yoon, "Challenges and Opportunities of Packaging FAB Near the End of Moore's Law," *IMAPS*, October 2021.